Please check that this question paper contains 09 questions and 02 printed pages within first ten minutes.

[Total No. of Questions: 09] [Total No. of Pages: .....]

Uni. Roll No. .....

Program: B.Tech. (Batch 2018 onward)

Semester: 3rd

Name of Subject: Digital Electronics

Subject Code: ESCS-101

Paper ID: 16012

Scientific calculator is not allowed.

MORNING

10 MAY 2023

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1. (a) Solve $(85.63)_{10}$ into $(X)_2$

(b) Interpret the concept of Duality principle with an example.

(c) What is Race around condition? How it can be avoided?

(d) Find the value of x in $(327)_x = (215)_{10}$

(e) Differentiate between level and edge triggering.

(f) List the various advantages of ring counter?

Part – B **[Marks: 04 each]**

Q2. Explain the working and truth table of J-K flip flop in detail.

Q3. Compare and contrast Synchronous counter and Asynchronous counter?

Q4. Translate **C'D+ABC'+A'B'D+ABD'** into standard POS form.

Q5. Design a Combinational circuit which has four inputs and one output. The Output is equal to 1 when following conditions meet:

(a) All the inputs equal to 1

(b) None of the inputs equal to 1

(c) An odd number of inputs equal to 1.

Q6. Minimize the given expression using K-Maps. **$f = \Sigma m$ (0, 4, 7, 8, 9, 10, 11, 16, 24, 25, 26, 27, 29, 31).**

Q7. Explain block diagram of encoder to explain its functions.

Part – C **[Marks: 12 each]**

Q8. Construct a 4-bit Binary to Gray Code Converter with proper truth table, K-Maps and Circuit Diagram Implementation.

OR

Illustrate the advantages and disadvantages of RTL, DTL, and TTL logic families.

Q9. Design a 4-bit synchronous counter using J-K flip flops to count the following sequence 0, 3, 5, 9, 11, 14.

OR

Explain the following in detail:

(a) Programmable Logic Array (PLA),

(b) Programmable Array Logic (PAL),

(c) Field Programmable Gate Arrays (FPGA).

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